UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/760,405	01/12/2001	Xiaoning Nie	GR 00 P 1031	1766

7590 01/13/2004

LERNER AND GREENBERG, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480

EXAMINER	
O'BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	7

DATE MAILED: 01/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/760,405	NIE, XIAONING	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 1/12/01,2/16/01,4/4/01,2/13/02,7/30/02.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5, 6.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-12 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Declaration as received on 4/4/2001, Priority Papers as received on 2/16/2001, IDS as received on 2/13/2002 and IDS as received on 7/30/2002.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The abstract of the disclosure is objected to because it deals mostly with the purported merits or speculative applications of the invention, rather than the invention as claimed. Correction is required. See MPEP § 608.01(b).

6. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves

modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Claim Objections

7. Claim 9 is objected to because of the following informalities: The claim recites the language "a first multiplexer writing either the output signal of said adder or the addresses for program jumps or function calls into said program counter assigned to the active process." A "de-multiplexer" more generally performs the operation described in this language, as it is not selecting one out of the two inputs as a multiplexer conventionally does, but is rather selecting between two inputs to be output to one of many outputs. Please correct the claim language to reflect the appropriate hardware component for this operation. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

10. Regarding claim 1, the claim language recites, "a program memory having stored therein at least one compiled program with a multiplicity N of independent processes, the compiled program including information on parallelism and a multiplicity of bundles with a plurality of instructions of a process." It is unclear whether the "multiplicity of bundles" are included within the compiled program, or whether there is only "information" included on the multiplicity of bundles. Please correct the claim language to more clearly point out the claimed invention and its operation. For the purposes of this examination, it is assumed that the compiled program contains a multiplicity of bundles, bundles that contain a plurality of instructions belonging to a process.

11. Further regarding claim 1, the claim language recites, "a program flow control unit connected to said branching control unit, said program flow control unit controlling a fetching of bundles from said program memory and said branch control unit and an output of instruction in dependence on information contained in the instructions and included in a compiling time of the program." It is unclear whether the program flow control unit is controlling the branch control unit claimed here, or whether bundles are being fetched from the branch control unit. Similarly, it is unclear whether the program flow control unit is controlling the output of instructions as claimed, of whether bundles are being fetched from the outputted instructions. Please correct the claim language to more clearly point out the claimed invention and its operation. For the

purposes of this examination, it is assumed that the program flow control unit is controlling both the branch control unit, and the outputting of instructions.

12. Regarding claim 7, the parent claim of claim 7 describes the program flow control unit as fetching instructions from the program memory and outputting instructions based on their dependence. The specification cites on pages 8 and 14 that the execution units (19 and 20 of Fig.1) execute bundles of instructions in parallel. However, claim 7 recites that the program flow control unit is executing bundles of instructions in parallel, while Fig.1 shows the program flow control unit situated before instructions are even issued to the execution units, which, along with convention, would suggest that the program flow control unit does not execute the bundles of instructions, but that the parallel execution units do. It is unclear then whether the program flow control unit executes bundles of instructions, the execution units execute bundles of instructions, or both. Please correct the claim language and/or the specification to more clearly define how execution of bundles occurs. For the purposes of this examination, in order to align with convention and the specification, it will be assumed that the execution units execute bundles of instruction in parallel.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

14. Claims 1-8 and 10 are rejected under 35 U.S.C. 102(a) as being anticipated by Gupta et al., U.S. Patent No. 5,941,983.

15. Regarding claim 1, Gupta has taught a data processing device for processing in parallel a plurality of independent processes, comprising:

a. A program memory (78 of Fig.3) having stored therein at least one compiled program with a multiplicity N of independent processes, the compiled program including information on parallelism and a multiplicity of bundles with a plurality of instructions of a process (see Col.6 lines 4-14),

b. A branching control unit (80 of Fig.3) connected to and addressing said program memory (see Col.9 lines 44-52). Here, because the instruction fetch units are fetching instructions from the instruction queues, they are inherently addressing the program memory in order to read out instructions from it.

c. A register (88 of Fig.3) for storing flags and data which are switched in dependence on a process being executed (see Col.8 lines 57-60 and Col.9 lines 62-65),

d. A program flow control unit (80 of Fig.3) connected to said branching control unit, said program flow control unit controlling a fetching of bundles from said program memory and said branching control unit and an output of instructions in dependence on information contained in the instructions and included in a compiling time of the program (see Col.9 lines 44-52).

16. Regarding claim 2, Gupta has taught the data processing device according to claim 1, which comprises a number N instruction buffers (see 94a-c of Fig.3) connected in parallel

downstream of said program memory for storing instructions read out from said program memory (see Fig.3).

17. Regarding claim 3, Gupta has taught the data processing device according to claim 2, which comprises an instruction output selector (80 of Fig.3) connected to and controlled by said program flow control unit such that said instruction output selector reads out instructions from said instruction buffers and outputs N instructions in parallel (see Col.9 lines 44-62).

18. Regarding claim 4, Gupta has taught the data processing device according to claim 1, which comprises N instruction decoders (80 of Fig.3) for decoding the instructions being output (see Col.9 lines 44-52).

19. Regarding claim 5, Gupta has taught the data processing device according to claim 1, comprising at least two instruction-execution units (84 of Fig.3) for outputting the N decoded instructions.

20. Regarding claim 6, Gupta has taught the data processing device according to claim 5, which comprises a data memory (86 of Fig.3) and at least two buses connecting said N instruction-execution units to said data memory (see connections between 84 and 86 of Fig.3).

21. Regarding claim 7, Gupta has taught the data processing device according to claim 1, wherein said program flow control unit is configured to execute the instructions of one or more bundles in parallel (see Col.1 line 55 – Col.2 line 9, Col.6 lines 39-55, and Col.10 lines 20-26).

22. Regarding claim 8, Gupta has taught the data processing device according to claim 1, wherein said branching control unit is configured to output an address pointer for addressing a bundle (see Col.9 lines 44-52). Here, because the instruction fetch units are fetching instructions from the instruction queues to be executed in parallel using instruction pointers (see Col.20 lines

22-33), and because they are fetching multiple independent instructions simultaneously using the instruction pointers, they are inherently outputting instruction pointers to address the multiple independent instructions (bundles).

23. Regarding claim 9, Gupta has taught the data processing device according to claim 1, but has not explicitly taught wherein the branching control unit comprises:

a. A first multiplexer and a second multiplexer. While not taught explicitly, the function of two multiplexers is inherent in the operation of the circuit (see paragraphs (e), (f), and (g) below).

b. An adder. Here, Gupta has taught the use of a PC counter distance encoded in an instruction to update the PCs for each individual thread (see Col.20 lines 22-33). Because a PC counter distance or an absolute new address can be encoded for branch instructions (see Col.20 lines 39-51), as well as the next sequential fetch address as long as the encoded dependencies for non-branch instructions are satisfied (see Col.6 lines 51-55 and Col.10 lines 6-26), there is inherently an adder so that the offset, whether branch offset or a sequential offset, can be added to the threads PC to create a new target address.

c. N program counters. Here, Gupta has taught each thread having its own instruction queue with corresponding program counter (see Col.6 lines 4-14 and Col.20 lines 26-32),

d. Wherein said program flow control unit feeds a number of instructions in a bundle to said adder and said adder adds an address pointer and the number of instructions. Here, Gupta has taught

e. Wherein said program flow control unit feeds addresses for program jumps or function calls and a process number to said first multiplexer. Here, Gupta has taught the location in each thread that a branch instruction may jump to being encoded in an instruction, and then updating the PC associated with each thread with this new PC value (see Col.20 lines 22-32). Therefore, the circuit is inherently operating as a de-multiplexer, selecting a PC to write the jump address into based upon the thread the instruction is part of.

f. Said first multiplexer writing either the output signal of said adder or the addresses for program jumps or function calls into said program counter assigned to the active process. Here, Gupta has taught the instruction location in each thread that a branch instruction may jump to being encoded in an instruction, and then updating the PC associated with each thread with this new PC value if needed (see Col.20 lines 39-51), or an offset to a PC value may be used which requires the output of the adder as described above (see Col.20 lines 22-32). Therefore, the circuit is inherently operating as a de-multiplexer, selecting a PC to write the jump address, whether absolute or an offset, into based upon the thread the instruction is part of.

g. A content of said program counter assigned to the currently active process is output as a new address pointer via said second multiplexer which is controlled using the process number supplied. Here, Gupta has taught that multiple threads can be active at once, that each thread has its own PC and corresponding functional unit, thus allowing parallel execution of threads (see Col.6 lines 4-14

and Col.20 lines 22-32). Therefore, the circuit described by Gupta inherently operates as a multiplexer, selecting and outputting a PC to be executed from based on its associated thread.

24. Regarding claim 10, Gupta has taught the data processing device according to claim 1, wherein said program flow control unit is configured to receive via a subbus of an output bus of said program memory at least one of the following:

a. At least one bit for indicating the parallel execution of instructions,

b. At least one bit for indicating the length of the following instruction bundle,

c. The indication of one or more NOPs in the instruction bundles,

d. A priority of the processes of the instructions.

25. Here, Gupta has taught the encoding of dependency information within instructions, with the dependency information being a number of bits identifying a dependent instruction by giving its location (see Col.10 lines 6-19 and Fig.8). Because this information identifies instructions that cannot be executed in parallel, these bits can be considered to be an indication of an instructions ability to execute in parallel with another instruction, provided that it is not encoded as a dependent instruction. Because the claim is written in the alternative format, and Gupta meets one of the four options, the claim language is satisfied.

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta et al., U.S. Patent No. 5,941,983 as applied to claim 1 above, and further in view of Ito et al., U.S. Patent No. 5,742,782.

28. Regarding claim 11, Gupta has taught the data processing device according to claim 1, but has not explicitly taught wherein a process is called by assigning a process number, a priority and a memory address of a starting point of the process in the program memory.

29. However, Ito has taught the selection of a process using an instruction stream number (see "STN" of Fig.13 and Col.10 lines 50-51), a priority based on whether a NOP instruction is referenced in the instruction stream (see "Signal155" of Fig.13 and Col.11 lines 9-13, 21-24), and the address of the thread starting point (see Col.10 lines 31-41) in order to more efficiently schedule threads and more effectively use a processor's parallel processing capabilities (see Col.3 lines 32-36). One of ordinary skill in the art would have recognized the desire in microprocessor design to make a design more efficient, thus saving important processor resources. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Gupta to include the selection of a thread based on assigning it a process number, a priority, and providing a memory address of the beginning of the process in order to more efficiently and effectively use the processor's parallel processing capabilities.

30. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta et al., U.S. Patent No. 5,941,983 as applied to claim 1 above, and further in view of Allen, Jr. et al., U.S. Patent No. 6,404,752.

31. Regarding claim 12, Gupta has taught the data processing device according to claim 1, but has not explicitly taught wherein said data processing device is a network processor for processing layer 1 to 7 of protocol stacks in applications including LAN, ATM switches, IP routers, and frame relays based on a system selected from the group consisting of DSL, Ethernet, and cable modems.

32. However, Allen, Jr. has taught the use of general-purpose microprocessors as network processors to provide a cost-effective solution to processing protocol stack layers for IDSN, cable and DSL modems, that provides high throughput and speeds (see Col.1 lines 44-49 and Col.2 line 38 – Col.3 line 23). One of ordinary skill in the art would have recognized that a primary goal in microprocessor design is to lower costs while maintaining a high level of performance. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Gupta to be used in a network processor because Gupta has taught a high-performance, general-purpose processor (see Col.5 lines 62-65), thus allowing costs to be kept low while providing a high level of network processing performance.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

34. Kahle et al., U.S. Patent No. 5,913,925 has taught a method and system for executing multi-threaded programs on a processor using embedded thread descriptors.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
1/8/2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100